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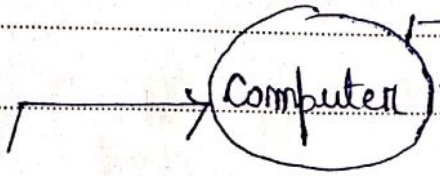
Date: 09/03/2020

Memory Interfacing. [COA]

(1)



Data + Program

(M/c) language [0's and 1's]

Representation:

1 bit = [0] or [1] — 2

2-bit = 00, 01, 10, 11 — 4

k-bits ---------- 2^k possibilities

Q1 A digital system has 986 possibilities. What will be the minimum bits required to represent these possibilities —

Ans: 2^{10}.

[10-bits]

Units:

1 bit ⟶ 0 or 1

8 bit ⟶ 1 byte

1024 bytes ⟶ 1KB

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1024 KB ⟶ 1MB

1024 MB ⟶ 1GB

Computer Architecture:

(CA)

↳ It deals with (Internal Design) ⟵ { Instructions, Addressing modes, ALU, Pipelining }

Computer Organization:

It deals with how various Memories and I/O Interact with a system.

Computer Design:

It deals with the hardware design

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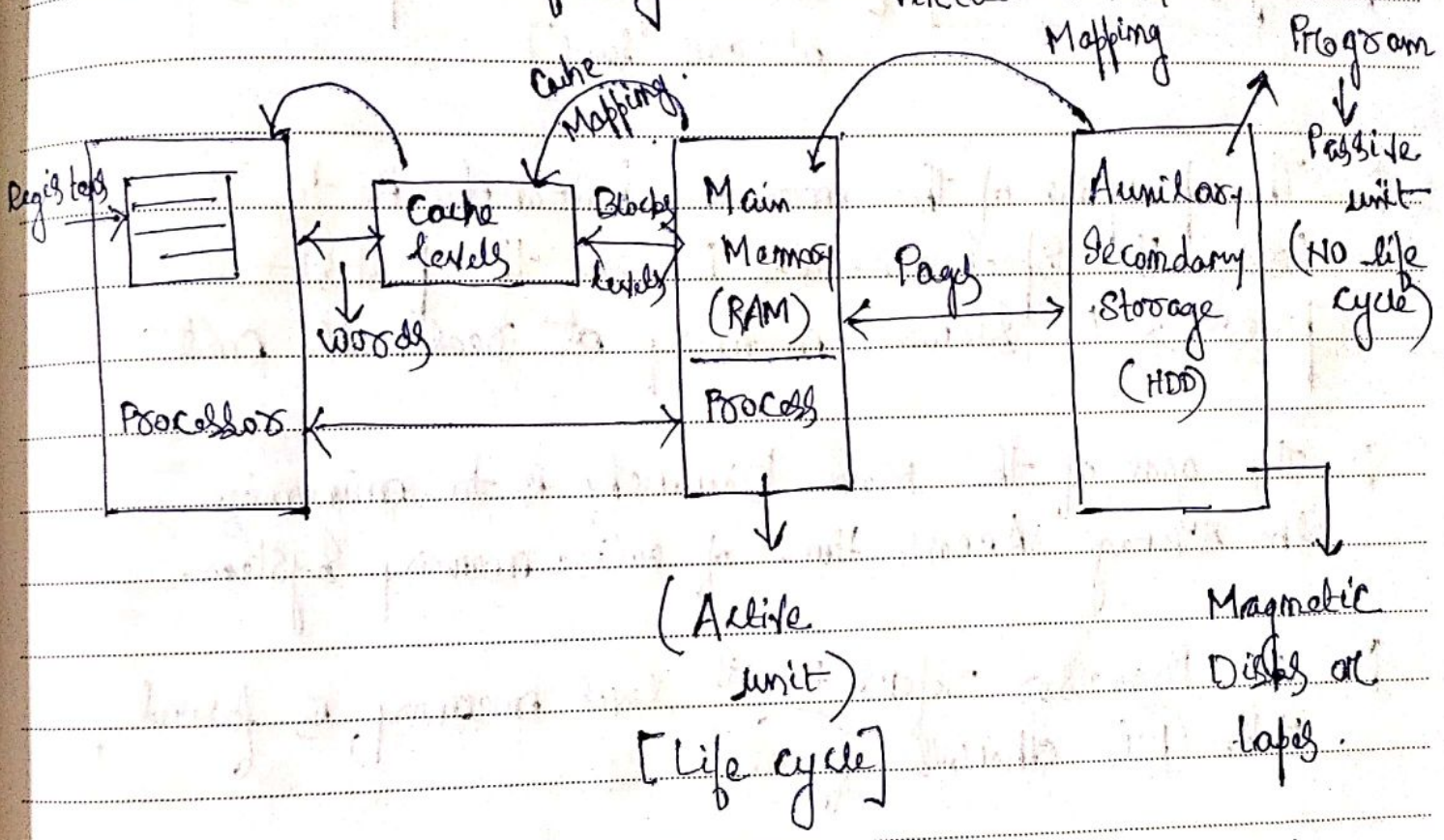
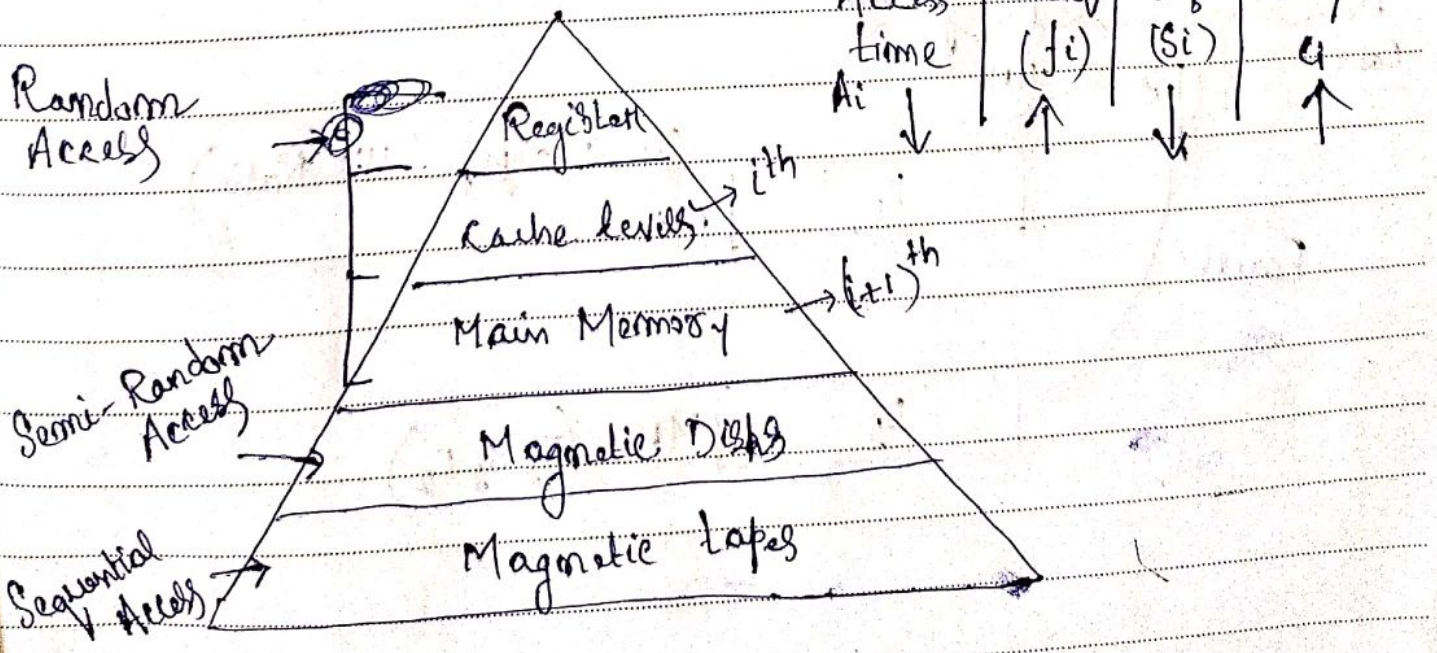
COA.

Basic Model of Memory Interfacing:





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▷ [ith ⊂ (i+1)th] [Some information present at each level]

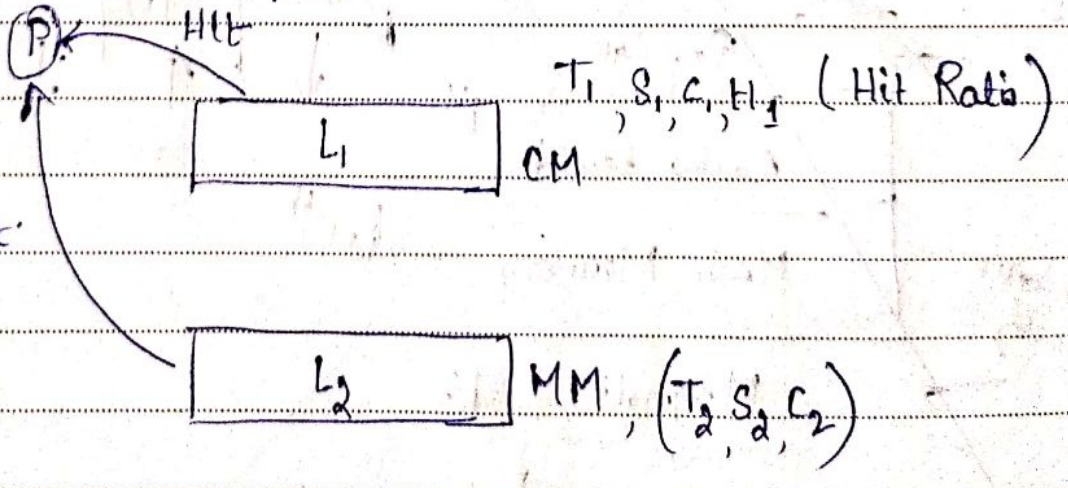
▷ The purpose of the memory hierarchy is to bridge the speed mismatch between the fastest processor to slowest memory at reasonable cost

▷ The goal of the Mem. hierarchy is to minimize the Average Access time of entire memory system.

▷ If Processor refers to ith level memory, is found, then (hit) otherwise (fault).

2- Level Memory System:

Case 1



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$$T_{avg} = H_1 \times T_1 + (1 - H_1)\, T_2$$

$$C_{avg/bit} = \frac{C_1 S_1 + C_2 S_2}{S_1 + S_2}$$

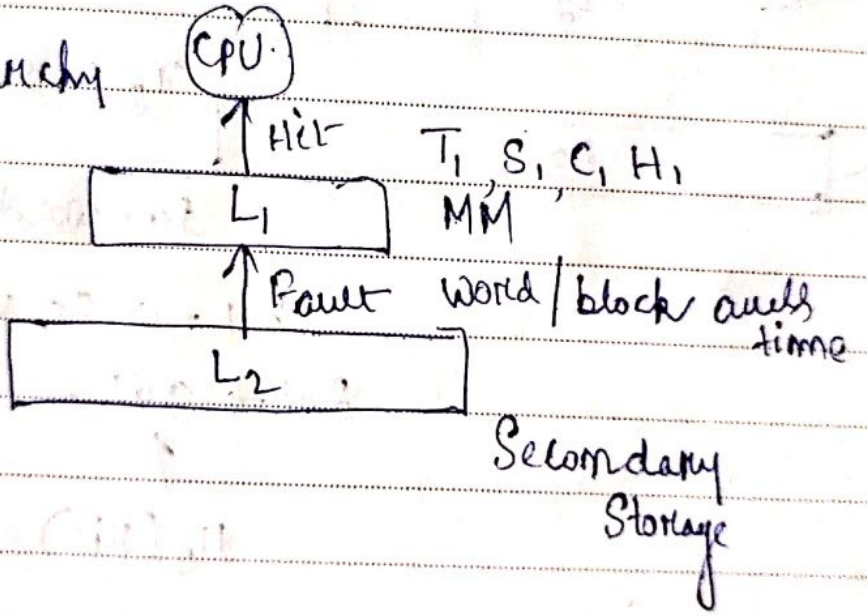
T_i : Access time of level i

S_i : Size of level i

C_i : Cost per word in ith level

H_i : Hit Ratio in level i

Case 2 Strict Hierarchy



$$T_{avg} = H_1 \times T_1 + (1 - H_1)\,(T_2 + T_1)$$

$$C_{avg/bit} = \frac{C_1 S_1 + C_2 S_2}{(S_1 + S_2)}$$

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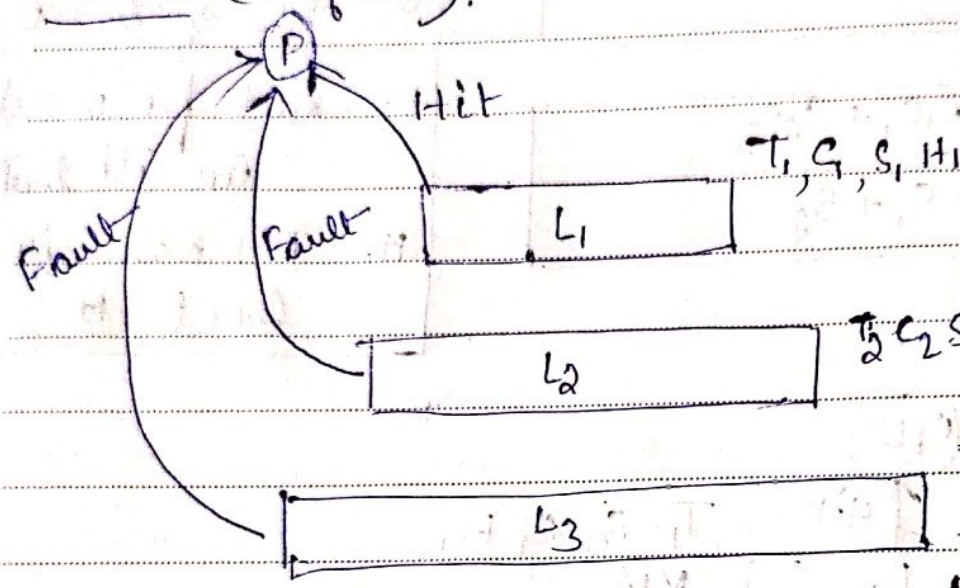
3-Level Memory System:

Case 1: (Default):



100 words

80% → 80 words → L_1 (Hit)

20% → 90% → L_2 → 18 words

H_2 (Hit) ⇒ L_3 → 2 words

$$T_{avg} = H_1 \times T_1 + (1-H_1) H_2 \times T_2 + (1-H_1)(1-H_2) \times T_3$$

$$C_{avg/bit} = \frac{C_1 S_1 + C_1 S_2 + C_3 S_3}{S_1 + S_2 + S_3}$$

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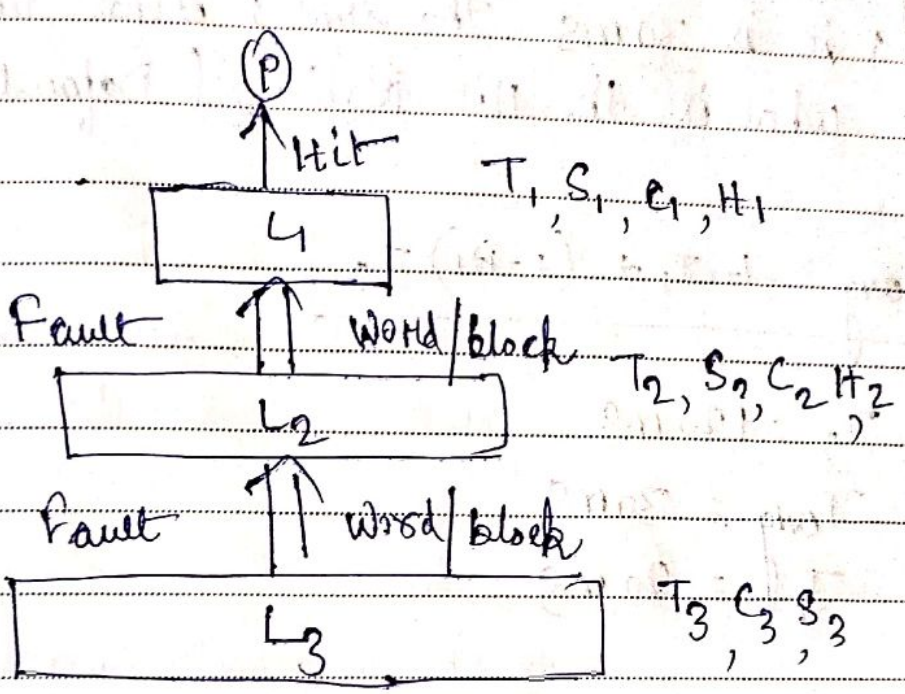
Case 2: (Strict Hierarchy):



$$T_{avg} = H_1 \times T_1 + (1-H_1) H_2 \times (T_2 + T_1) + (1-H_1)(1-H_2)(T_3 + T_2 + T_1)$$

$$C_{avg/bit} = \frac{C_1 S_1 + C_2 S_2 + C_3 S_3}{S_1 + S_2 + S_3}$$

Q1: Consider a 2-level memory system in which the average access time without level-1 is 120ms, with level-1 it is 30ms. The level-1 access time is 20ms. What is the Hit Ratio. (Default organization)

$\Rightarrow$ $\boxed{T_{avg} = H_1 T_1 + (1-H_1) T_2}$

$T_2 = 120\ ms$

$T_{avg} = 30\ ms$

$T_1 = 20\ ms$

$30 = H_1 \times 20 + (1-H_1) \times 120.$

$\Rightarrow 100H_1 = 90.$

$\Rightarrow H_1 = \frac{90}{100} = 0.9$

$\therefore$ $\boxed{\text{Hit Ratio} = 0.9}$

Q2: Consider a two level Memory System where the access time of level-1 and level-2 memories are — 10 ms and 150 ms, what is the avg. access time, if L_1 has hit ratio. 90%.

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H_1 T_1

$$T_{avg} = (0.9) \times 10 + (1-0.9) \times 150.$$

$$= 9 + 15 = \boxed{24ms}$$

Q3] A System is employing with 2-levels. The avg access time w/o level-1 is 150ms and with level 1 is 30ms. The level-1 access time is ~~25ms~~ 20ms

(i) If Hit Ratio is made to 100%, what will be the access time of L_1 and L_2.

Ans: (i) Note: The Hit Ratio does not influence the access time of L_1 and L_2 memories

$\therefore T_1 = 20ms \quad T_2 = 150ms$

The $\boxed{T_{avg}}$ value will change.

(ii.) If T_{avg} is increased by 10%, what is the percentage of change in the hit Ratio.

$$\text{Hit Ratio} \propto \frac{1}{T_{avg}}$$

$$T_{navg} = 30 + 10\% \text{ of } 30.$$

$$= 30 + 3 = 33$$

$$\therefore 33 = H_1 \times 20 + (1 - H_1) \times 150.$$

$$\Rightarrow 33 = 150 - 130 H_1$$

$$\Rightarrow H_1 = \frac{117}{130} = 90\% = \underline{2.33\%} \text{ decreased.}$$

Q4 At 0.8 hit in level-1 memory, the average access time is increased by 20% from 60 ns. The (4) memory is (5) times faster than L_2. What is the percentage of change in the Hit Ratio —

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$T_{avg\_old} = 60\ ms$

$T_{avg\_new} = 60 + 20\%.0 \mid 60.$

$= 60 + \frac{20}{100} \times 60$

$= 72$

$\rightarrow \quad 60 = 0.8 \times T_1 + 0.2\, T_2$

$\Rightarrow \quad 60 = 0.8 \times T_1 + 0.2 \times (5 \times T_1)$

$\Rightarrow \quad T_1 = 33.33$

$\therefore \quad 72 = H_1 * 33.33 + (1 - H_1) \times 5 \times 33.33$

$\Rightarrow \quad 72 = 33.33 H_1 + (1 - H_1) \times 166.66\ ms$

$\Rightarrow \quad 72 = 166.66 - 133.33 H_1$

$\Rightarrow \quad H_1 = \frac{94.66}{133.33} = 10\% \downarrow$

Q5 Consider a system with two level cache —

Access time of L_1 = 1 ms

Access time of L_2 = 10 ms

Access time of Main Memory = 500 ms

The Hit Rate of (L1) and (L2) caches are 0.8 and 0.9. What is the T_{avg} ignoring the searched time within the cache ? (Default cache organization)

Ans:

$$T_{avg} = 0.8 \times 1 + (1-0.2) \times 0.9 \times 10 + (1-0.2)(1-0.9) \times 500$$

$$= 0.8 + 1.8 + 10$$

$$= 12.6 \text{ ms}$$

Q6 A system is employing with 3-levels. The Access time of L_1, L_2 and L_3 memories is 10 ms/word, 150 ms/word and 500 ms/word. The L_2 and the L_3 memories are divided into a block of 5 words. When a page fault occurs in (L1) or (L2) the processor must read from L_3 memory only — The H_1 and H_2 are 80% and 90%. What is T_{avg}

Ans:

$T_1 = 100\,ms$

$T_3 = 500 \times 5 = 2500\,ms$

$T_2 = 150 \times 5 = 750\,ms$

$$T_{avg} = 0.8 \times 100 + 0.2 \times (0.9)(500+750) + (0.2) \times (0.1) \times (100+750+2500)$$

$$= 80 + 153 + 67$$

$$= 300\,ms$$